Influence of Oxygen Diffusion Through Capping Layers of Low Work Function Metal Gate Electrodes

Bei Chen, Rashmi Jha, Heather Lazar, Nivedita Biswas, *Member, IEEE*, Jaehoon Lee, Bongmook Lee, Leszek Wielunski, Eric Garfunkel, and Veena Misra, *Senior Member, IEEE*

***Abstract*—This letter evaluates Ru and W capping layers for MoTa metal gate electrodes in MOS capacitor applications. The authors report that the oxygen diffusion from the capping layer plays an important role in determining the MoTa alloy effective work function value on SiO_2. A MoTa alloy metal gate with Ru capping exhibits stable effective work function up to 900 °C annealing but is not stable with W capping. Auger electron spectroscopy and Rutherford backscattering spectroscopy analyses show minimal oxygen diffusion into MoTa gate stacks with Ru capping while severe oxygen diffusion into the gate is observed with W capping metal after 900 °C annealing. Current–voltage analysis also demonstrates different barrier heights of MoTa on SiO_2 with Ru or W capping layer after 900 °C annealing, confirming the effective work function value change.**

***Index Terms*—Alloy, capping, effective work function, metal gate, MoTa, oxygen diffusion.**

I. Introduction

METAL gates on high-κ dielectrics are being considered as replacements for polycrystalline silicon to eliminate gate depletion effects for CMOS devices with gate lengths below 50 nm [1], [2]. Metal gates can also eliminate poly-Si boron penetration and higher threshold voltages associated with Fermi level pinning [3]. To achieve low threshold voltages, the effective work function (Φ_m) for NMOS and PMOS gates must be near 4 and 5 eV, respectively [4]. It has recently been shown that oxygen at the metal gate and dielectric interface can modify the metal gate Φ_m [5], [6] due to the formation of interface dipoles and/or reactions layers. Recently, it has been shown that the MoTa alloy capped with Ru exhibited low Φ_m and good thermal stability on SiO_2 [7]. Ru and W have both been considered as metal electrodes and capping layers [8]–[10]. In this letter, we have compared the oxygen diffusion in MoTa with Ru and W capping layers. It was found that both Φ_m and the equivalent oxide thickness (EOT) are strong functions of the capping layer. This suggests that the capping layer is a critical component of the gatestack, which needs to be optimized concurrently with the rest of the gatestack. This understanding is critical for low work function metals that have high affinity toward oxygen and as such are thermally unstable on dielectrics.

Manuscript received September 30, 2005; revised December 15, 2005. The review of this letter was arranged by Editor A. Chatterjee.

B. Chen, R. Jha, H. Lazar, N. Biswas, J. Lee, B. Lee, and V. Misra are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA (e-mail: vmisra@ncsu.edu).

L. Wielunski and E. Garfunkel are with the Department of Chemistry and Chemical Biology, Rutgers–The State University of New Jersey, Piscataway, NJ 08854 USA.

Digital Object Identifier 10.1109/LED.2006.871184

II. Experimental

Thermally grown SiO_2 at 900 °C with thicknesses of 30–90 Å were used as gate dielectrics. The MoTa gate electrodes were deposited by cosputtering Mo at 70 W and Ta at 100 W in an RF magnetron sputtering system. An *in situ* 500 Å Ru or W capping layer was deposited by sputtering Ru or W on the MoTa alloy gate. All samples were subjected to a forming gas anneal (FGA) at 400 °C for 30 min prior to characterization. To evaluate the thermal stability, the samples were subsequently rapid thermal annealed (RTA) in Ar at 900 °C for 15 s after the FGA. The oxygen depth profile in the gate stack was obtained using Auger electron spectroscopy (AES) and 2 MeV He Rutherford backscattering spectroscopy (RBS). Capacitance–voltage $(C–V)$ and current–voltage $(I–V)$ characteristics were obtained using HP4284 LCR meter and HP4155, respectively. The flatband voltage $(V_{\rm fb})$ and the EOT for the capacitors were obtained by using the NCSU CV program [11].

III. Results and Discussion

Fig. 1 shows $V_{\rm fb}$ versus EOT of the MoTa alloy on SiO_2 at different anneal temperatures (400 °C and 900 °C) with Ru and W capping. An Ru capping layer results in stable properties at high temperatures, whereas a W capping layer suffers from large changes in Φ_m and EOT. The Φ_m of the MoTa gate was determined using the flatband voltage $(V_{\rm FB} = \Phi_m - \Phi_S - Q_F(\mathrm{EOT}/\varepsilon_{\rm ox}))$, where Φ_S and Q_F represent the work function of the Si substrate and the fixed charge at the Si–dielectric interface [12]. With a Ru cap, the MoTa gate Φ_m was 4.16 and 4.32 eV at 400 °C FGA and 900 °C RTA, respectively. A small change in EOT of 1–2 Å was observed with different anneals. However, with a W cap, the Φ_m of MoTa increased from 4.12 eV at 400 °C FGA to 4.68 eV after 900 °C RTA. In addition, an EOT increase of $\sim$ 10 Å was also observed after 900 °C RTA. In order to verify that the Φ_m change was not related to the charges at the electrode–dielectric interface, barrier heights (ϕ_b) were obtained by using Fowler–Nordheim tunneling analysis [13]. Fig. 2 shows the $I–V$ curves of MoTa

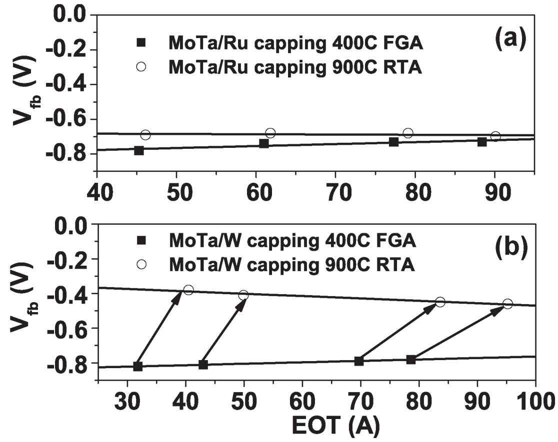

Fig. 1. V_{fb} versus EOT curves of (a) MoTa/Ru and (b) MoTa/W at 400 °C FGA and 900 °C RTA. The MoTa/Ru stack has stable work function values up to 900 °C, while the work function and EOT of MoTa/W increase after 900 °C RTA.

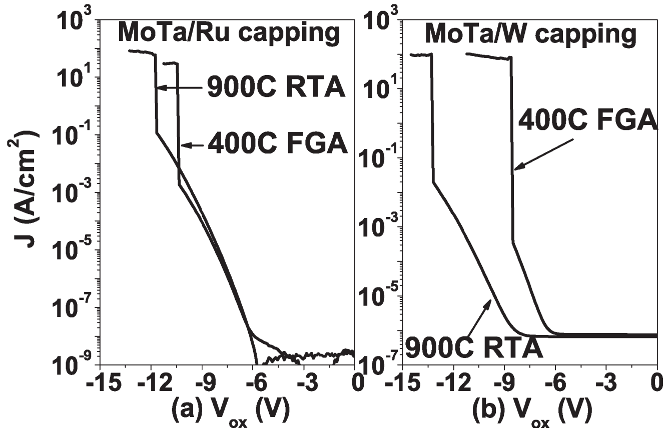

Fig. 2. I–V curves of (a) MoTa/Ru and (b) MoTa/W at 400 °C FGA and 900 °C RTA, showing that MoTa/Ru has a similar I–V at 400 °C FGA and 900 °C RTA, whereas the I–V curve of MoTa/W shifts to lower values after 900 °C RTA.

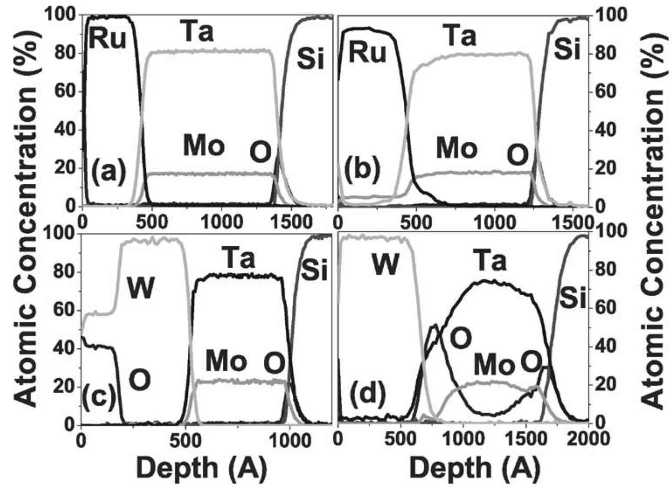

Fig. 3. AES depth profiling of (a) MoTa/Ru at 400 °C FGA, (b) MoTa/Ru at 900 °C RTA, (c) MoTa/W at 400 °C FGA, and (d) MoTa/W at 900 °C RTA. MoTa/Ru has a sharp interface with SiO_2 at both 400 °C FGA and 900 °C RTA, indicating good thermal stability. MoTa getters oxygen from WO_x at 900 °C RTA. WO_x forms during the 400 °C FGA.

alloy on SiO_2 with an Ru or W cap at different anneal temperatures (400 °C and 900 °C). The Ru caps were found to have similar gate currents at both temperatures with a ϕ_b of 3.3 eV at 400 °C FGA and 3.4 eV at 900 °C RTA. However, the W-capped samples had a ϕ_b of 3.3 eV at 400 °C FGA, which increased to 3.8 eV after 900 °C RTA. In addition, the gate currents decreased after RTA owing to the EOT increase. In both cases, the extracted ϕ_b values matched well with the CV-extracted Φ_m values, confirming that Ru and W capping have a drastically different impact on the electrical properties of MoTa gates.

In order to further understand the differences in these two capping layers on MoTa gates, the oxygen diffusion behavior was studied. Fig. 3(a) and (b) shows the AES depth analysis of MoTa gate with Ru capping at 400 °C and 900 °C, respectively. Some intermixing between the Ru capping layer and the MoTa gate is observed, but the MoTa and SiO_2 interface remains abrupt, indicating minimal intermixing between the MoTa alloy and the dielectric after a 900 °C RTA. No oxygen is detected in the gate electrode or in the Ru capping layer except on the Ru surface, which oxidizes during 900 °C RTA. The RBS analysis also demonstrates that there is no metal diffusion into the Si channel after a 900 °C RTA. Fig. 3(c) and (d) shows the AES depth analysis of MoTa gate with W capping at 400 °C and 900 °C, respectively. Compared with the Ru capping layer, severe oxidation of the W capping layer occurs even at 400 °C FGA. As shown, approximately 200–300 Å of the surface of W oxidizes after FGA with $\sim$ 40% oxygen atomic composition when W oxidizes. However, from the AES analysis, there is no obvious oxygen diffusion into the MoTa gate at 400 °C FGA. After a subsequent 900 °C RTA, it was found that MoTa gettered the oxygen from the WO_x capping layer. The diffused oxygen piled up at the W/MoTa and MoTa/SiO_2 interfaces. There also exists about 8% oxygen in the MoTa layer from AES analysis. This is attributed to the high oxygen affinity of the low work function metals. The standard molar Gibbs energy of formation (ΔG_f) at 25 °C in kJ/mol of RuO_2 is -152.2 kJ/mol. ΔG_f of WO_3, MoO_3, and Ta_2O_5 are -764.0, -669.0 and -1911.2 kJ/mol, respectively [14]. Since there is no ΔG_f data for the MoTa alloy, the oxygen affinity for MoTa was estimated based on the Ta content of the film and was found to be much stronger than W. We attributed this as the primary reason that the MoTa alloy effectively getters the oxygen from the oxidized W layer at 900 °C. RBS analysis further revealed that two apparent interfacial layers were formed between the MoTa gate and SiO_2 after 900 °C RTA. The first layer, near the SiO_2, is a mixture of SiO_2 and Ta_2O_5 with composition $\sim Ta_{0.1}Si_{0.2}O_{0.7}$. T he se cond layer, near the MoTa gate, is a mixture of SiO_2, Ta oxide, and Mo oxide with approximate composition as $Mo_{0.09}Ta_{0.2}Si_{0.15}O_{0.56}$. Also, there exists $\sim$ 7% oxygen inside the MoTa alloy gate and 40% oxygen in the interfacial layer between the W cap and the MoTa alloy gate. Based on the above RBS data, we attribute the increase in EOT after RTA to the formation of Ta oxide (mixed with Mo and SiO_2). Due to Ta oxidation, a Mo-rich MoTa metal gate is left on the dielectric, which is expected to have a higher Φ_m due to the presence of either Mo and/or $MoSi_x$. This suggests that control of oxygen in metal gates via appropriate capping layers is critical in achieving low Φ_m since most low Φ_m metals tend to oxidize readily resulting in higher Φ_m values.

IV. Conclusion

Ru and W capping layers on the MoTa alloy gate were investigated by electrical and physical analyses. MoTa was stable with respect to Φ_m and EOT up to 900 °C with Ru capping layers. However, with a W capping layer, both Φ_m and the EOT of the MoTa alloy increased after 900 °C RTA. From AES and RBS analyses, we conclude that severe oxygen diffusion into the MoTa/W stacks is the reason for the thermal instability. This study suggests control of oxygen through capping layer optimization is necessary in achieving low work function gate electrodes that are thermally stable on dielectrics.

References

[1] G. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001.

[2] *International Technology Roadmap for Semiconductors*, S. I. Assoc., Austin, TX, 2004. [Online]. Available: http://public.itrs.net/

[3] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi level pinning at the polySi/metal oxide interface," in *VLSI Symp. Tech. Dig.*, 2003, pp. 9–10.

[4] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of gate workfunction on device performance at the 50 nm technology node," *Solid State Electron.*, vol. 44, no. 6, pp. 1077–1080, Jun. 2000.

[5] J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, and B. E. White, "Contributions to the effective work function of platinum on hafnium dioxide," *Appl. Phys. Lett.*, vol. 85, no. 10, pp. 1826–1828, Sep. 2004.

[6] D. Lim, R. Haight, M. Copel, and E. Cartier, "Oxygen defects and Fermi level location in metal–hafnium oxide–silicon structures," *Appl. Phys. Lett.*, vol. 87, no. 7, p. 072902, Aug. 2005.

[7] B. Chen, N. Biswas, and V. Misra, "Electrical and physical analysis of MoTa alloy for gate electrode applications," *J. Electrochem. Soc.* to be published.

[8] V. Misra, H. Zhong, and H. Lazar, "Electrical properties of Ru-based alloy gate electrodes for dual metal gate Si-CMOS," *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 354–356, Jun. 2002.

[9] D. A. Buchanan, F. R. McFeely, and J. J. Yurkas, "Fabrication of midgap metal gates compatible with ultrathin dielectrics," *Appl. Phys. Lett.*, vol. 73, no. 12, pp. 1676–1678, Sep. 1998.

[10] D.-G. Park, H.-J. Cho, K.-Y. Lim, T.-H. Cha, I.-S. Yeo, and J. W. Park, "Effects of TiN deposition on the characteristics of W/TiN/SiO_2/Si metal oxide semiconductor capacitors," *J. Electrochem. Soc.*, vol. 148, no. 9, pp. F189–F193, 2001.

[11] J. R. Hauser and W. T. Lynch, *SRC Working Paper*, 1997.

[12] Y. S. Suh, G. P. Heuss, and V. Misra, "Electrical characteristics of $TaSi_xN_y/SiO_2/Si$ structures by Fowler–Nordheim current analysis," *Appl. Phys. Lett.*, vol. 80, no. 8, pp. 1403–1405, Feb. 2002.

[13] Z. Weinberg, "On tunneling in metal–oxide–silicon structures," *J. Appl. Phys.*, vol. 53, no. 7, pp. 5052–5056, Jul. 1982.

[14] D. L. Lide, *Handbook of Chemistry and Physics*, 85th ed. New York: CRC Press, 2004.