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Advances in high κ gate dielectrics for Si and III–V semiconductors

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Abstract

Our ability of controlling the growth and interfaces of thin dielectric films on III–V semiconductors by ultrahigh vacuum deposition has led to investigations of gate stacks containing rare earth oxides of Gd_2O_3 and Y_2O_3 as alternative high κ gate dielectrics for Si. The abrupt interfaces achieved in these gate stacks have enabled the electrical, chemical, and structural studies to elucidate the critical materials integration issues for CMOS scaling, including morphology dependence, interfacial structure and reaction, thermal stability and gate electrode compatibility.

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1. Introduction

Nanoscale device technology is driving intense study of thin dielectric layers on semiconductors. The aggressive scaling of Si CMOS technology calls for identifying high κ dielectrics to replace SiO_2 and oxynitrides in gate related applications [1]. The fundamental material requirements for the alternative gate dielectric are very challenging in order to achieve performance comparable to SiO_2. These requirements include dielectric constant, band gap, conduction band offset, high recrystallization temperature (for amorphous dielectrics only), low oxygen diffusivity, thermodynamic stability in contact with Si at temperature exceeding 800°C, high quality interface with Si with low interfacial state density D_{it}, and lower leakage conduction than SiO_2 at an equivalent oxide thickness, t_{eq} less than 1.5 nm. Furthermore, there are demanding issues for process integration compatibility such as film morphology, interfacial structure and stability withstanding high temperature processing, and gate electrode compatibility and reliability [1,2]. The rare earth dielectric oxides

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have a high conduction band offset over 2 eV and show good thermodynamic stability in contact with Si, hence are considered as a very attractive candidate among several binary metal oxides currently in contention [3].

2. The discovery of $Ga_{2-x}Gd_xO_3$ and Gd_2O_3 dielectrics

Our interest in the rare earth oxide stems from our earlier work on GaAs passivation. The novel $Ga_{2-x}Gd_xO_3$ mixed oxides ($\kappa = 12$) grown by ultrahigh vacuum deposition from an oxide source formed an excellent insulating barrier with low interfacial state density D_{it} on the GaAs surface [4,5]. This discovery has led to the first GaAs based inversion channel metal-oxide-semiconductor field effect transistor (MOSFET) [6,7]. Subsequent studies have identified the important role of Gd_2O_3 in the $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$ dielectric films (GGG) for effective passivation of GaAs [8]. Additions of Gd with $x \geqslant 14\%$ were necessary to improve the dielectric performance, and help to stabilize the $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$ film chemically. Furthermore, for the MOS diodes with a low D_{it}, we found that the growth of the first few molecular layers of the $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$ oxides on GaAs contains only pure Gd_2O_3 [9]. A continued growth using GGG source led to the inclusion of gallium oxides in the films, thus forming the mixture of gallium and gadolinium oxides. Later, pure Gd_2O_3 oxides ($\kappa = 14$) film was discovered to grow epitaxially in an (1 1 0) oriented Mn_2O_3 crystal structure on the GaAs (1 0 0) surface, and formed an excellent insulting barrier for passivation [10]. Since then these two dielectrics have been successfully applied to other III–V semiconductors, including InGaAs, AlGaAs, InP, and GaN producing high quality MOS diodes and MOSFETs [11–13].

For Si CMOS applications we have studied Gd_2O_3 ($\kappa = 14$) and Y_2O_3 ($\kappa = 18$) dielectrics in both crystalline and amorphous phases as the alternative gate dielectrics replacing SiO_2 [14,15]. One unique aspect of our approach of ultrahigh vacuum evaporation of oxides is the ability of limiting the oxygen partial pressure to less than 10^{-9} Torr during growth, hence oxidation of the Si surface can be completely avoided. Unlike most other work reported, our oxide growth method by MBE has demonstrated the absence of SiO_2 or silicate common at the dielectric/Si interface, as characterized by infrared absorption spectroscopy (IRAS), medium energy ion scattering (MEIS), and scanning transmission electron miscopy (STEM) in conjunction with electron energy loss spectroscopy (EELS). The absence of interfacial layers represents a significant thickness saving for the overall dielectric layer. Although the MBE technique is not yet a proven technology for CMOS processing, the MBE grown amorphous-Si/Gd_2O_3/crystalline-Si and a-Si/Y_2O_3/c-Si gate stacks of abrupt interfaces served as a model system to elucidate critical integration issues including morphology dependence of electrical leakage, interfacial structure and reaction, thermal stability, and gate electrode compatibility.

3. Film morphology dependence

All dielectric films of Gd_2O_3, Y_2O_3, ZrO_2 were prepared by ultrahigh vacuum deposition on p-type (1 0 0) Si as previously described [14,15]. By systematically altering the film microstructure from two domain, single domain, weak epitaxial, to completely amorphous, we showed the dependence of leakage current density J_L on the dielectric film microstructure in Fig. 1. The crystalline Gd_2O_3 and Y_2O_3 films are grown in the (1 1 0) oriented Mn_2O_3 structure of two-fold symmetry on the (0 0 1) Si surface, and form two degenerate variants in the plane with equal probability [14,15]. Two fold degeneracy was effectively removed by the use of vicinal (0 0 1) Si substrates of 4° miscut toward $[1\,\bar{1}\,0]$. The attainment of single domain (1 1 0) Gd_2O_3 films and the elimination of domain boundaries have reduced the leakage current by 2–3 orders of magnitude compared to the mixed domain films. By depositions at a medium temperature $\sim$250°C we prepared weak epitaxial films consisting of small crystalline grains dispersed in an amorphous matrix. The amorphous dielectric films deposited at room temperature show impressively low leakages, about four orders of magnitude smaller than that in the crystalline

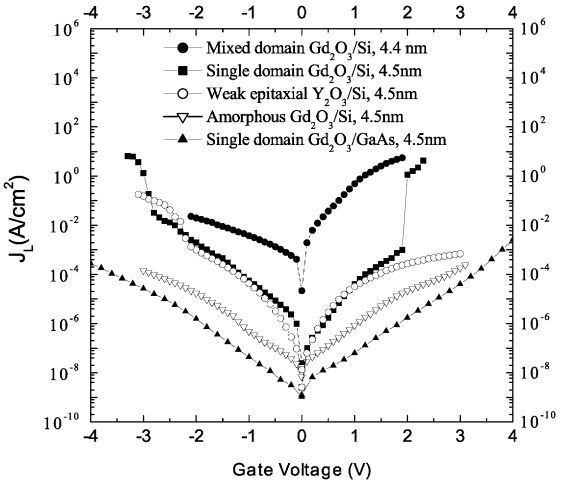

Fig. 1. Morphology dependence of leakage current density J_L vs. voltage for 4.5 nm Gd_2O_3 and Y_2O_3 films of varying microstructure on (1 0 0) Si and (1 0 0) GaAs.

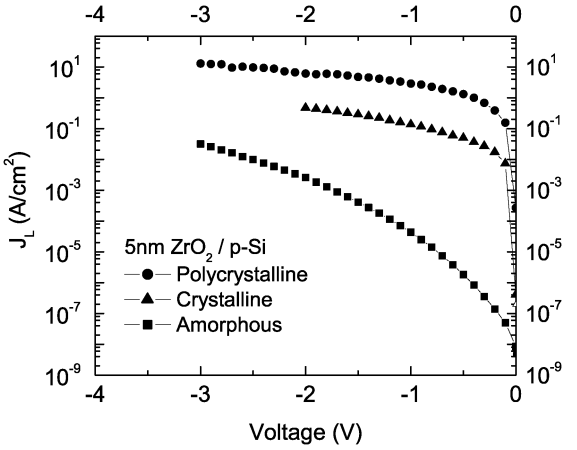

Fig. 2. Morphology dependence of leakage current density vs. voltage for 5.0 nm ZrO_2 fims of varying microstructure on (1 0 0) Si.

phase, and six orders of magnitude lower than that in SiO_2 with an equivalent oxide thickness, t_{eq}, of 1.0–2.0 nm, where t_{eq} is defined as $t(\kappa_{SiO_2}/\kappa_{oxide})$. The systematic reduction of leakage current density with decreasing film crystallinity suggested that grain boundaries as easy conduction pathways are the dominating factors giving rise to leakage. This further caused substantial variation of leakage currents among devices in a given wafer. The remarkably low leakage current of (1 1 0) epitaxial Gd_2O_3 film only 4.5 nm thick grown on (1 0 0) GaAs was also shown for comparison, with J_L at 1 V as low as 10^{-8} A/cm^2. This result demonstrate an excellent epitaxy taking place at this crystalline oxide/semiconductor interface virtually free of domain boundaries [9,10].

Our observation of the dependence of leakage on morphology is found not only in rare earth oxides, but also in another widely studied high κ dielectric ZrO_2 ($\kappa = 25$) shown in Fig. 2. At a substrate temperature of $\sim$500°C, the crystalline yttria ($\sim$15%) stabilized zirconia films grow epitaxially in the (1 0 0) cubic structure on (1 0 0) Si. Decreasing substrate temperature resulted in polycrystalline oxide films, and eventually led to completely amorphous films by room temperature deposition. Typical J_L at 1 V for amorphous ZrO_2 films 5.0 nm thick is 1.0×10^{-5} A/cm^2 with a t_{eq} of 1.0 nm.

4. Interfacial structure and hydroxide formation

A serious problem, however, is that rare earth oxides are know to be hygroscopic. That is, with increasing ionicity in binary oxides, reactions with water become a greater problem, leading to hydroxide formation after exposure of a thin film to atmospheric conditions. The interfacial reaction and stability of Y_2O_3 and Gd_2O_3 films with the Si substrate and with an in situ deposited amorphous Si capping layer were studied by MEIS using a 100 keV proton beam [16,17]. As shown in Figs. 3(a) and (b), the depth profiles of the elements (Si, O, Y) showed that uncapped films absorb excess *O* trapped in the form of water or hydroxide, and led to an oxygen composition ($Y_2O_{3.5}$) and the growth of an underlayer layer of SiO_xH_y and/or silicate 0.6–0.8 nm wide. Amorphous-Si-capped yttria layers prepared in UHV displayed stoichiometric (Y_2O_3) films, and exhibit an abrupt transition to the substrate less than 0.2 nm wide. The Si capping layer prevented the interfacial reaction with the Si substrate by blocking water or oxygen diffusion into the film. The trapped water or hydroxides in dielectrics resulted in undesirable frequency dispersions by about 30% from 1kHz to 1 MHz in the C-V data.

The cross section images of a-Si/Y_2O_3/c-Si a-Si/Gd_2O_3/c-Si gate stack were also examined by

STEM with EELS for chemical composition analysis [15,17]. The reactivity of rare earth oxides with water is a serious problem for TEM specimen preparation, as samples must be made very thin. The challenge is then to keep samples thick enough so that this reaction layer is a small fraction of the film thickness [17]. Fig. 4(a) is the annular dark field (ADF) image showing a sharp boundary and the absence of an interfacial layer with the Si substrate for a thick cross-section of a capped Y_2O_3 layer. Similar results were found in the capped Gd_2O_3/Si layer, and are consistent with the MEIS and IRAS findings [15,16,]. Fig. 4(b) reveals detection of a hydroxide SiO_xH_y layer in a thin cross-sectioned region of the same sample. The hydroxide phases for rare earth oxides can be readily detected by EELS as they generally result in a rounded O K-edge instead of the characteristic double-peak splitting expected for O bonded to transition metals [18]. As shown in Fig. 5, the EELS spectra of the (rounded) oxygen-K edge and the yttrium-$M_{4,5}$ edge indicate the presence of a yttrium free, SiO_xH_y interfacial layer extending about 0.6 nm in width near the Si substrate.

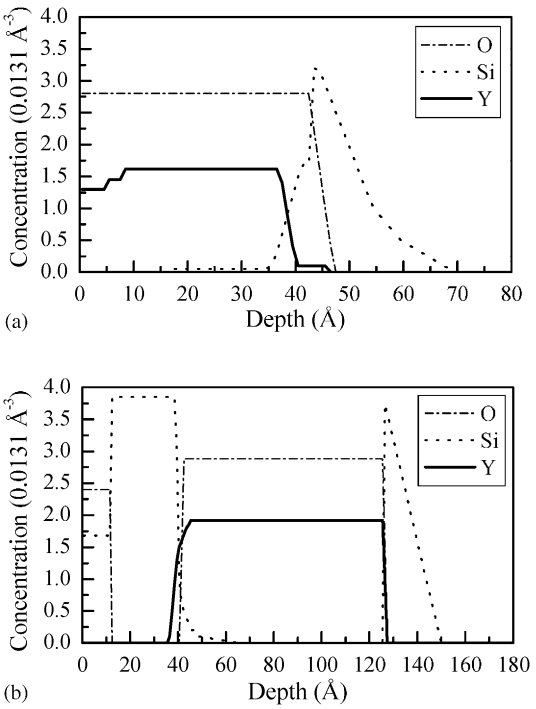

Fig. 3. MEIS depth profiles of O, Y, Si for amorphous Si (a) uncapped, and (b) capped Y_2O_3 layers.

5. Thermal stability and gate electrode compatibility

One of the critical tests for the high κ dielectrics is thermal stability withstanding high temperature processing. In situ vacuum anneals were performed during the MEIS measurements and showed that the uncapped yttria film annealed at 700°C resulted in Si uptake from the substrate into Y_2O_3, and formation of a silicate layer extending to about 1.5 nm in width [16]. In the amorphous-Si-capped gate stack, the interface of yttria to Si

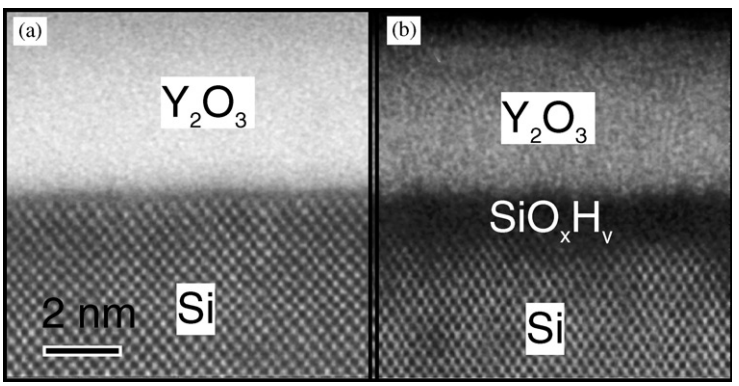

Fig. 4. (a) ADF-STEM image of an a-Si/Y_2O_3/c-Si stack, which is thick enough so that surface reaction layers are not visible. (b) The same a-Si/Y_2O_3/c-Si sample in a thinner region. Not only has a hydroxide formed on the entrance and exit surfaces, but the capping layer has also been milled away and the hydroxide reaction layers dominate the interface contrast.

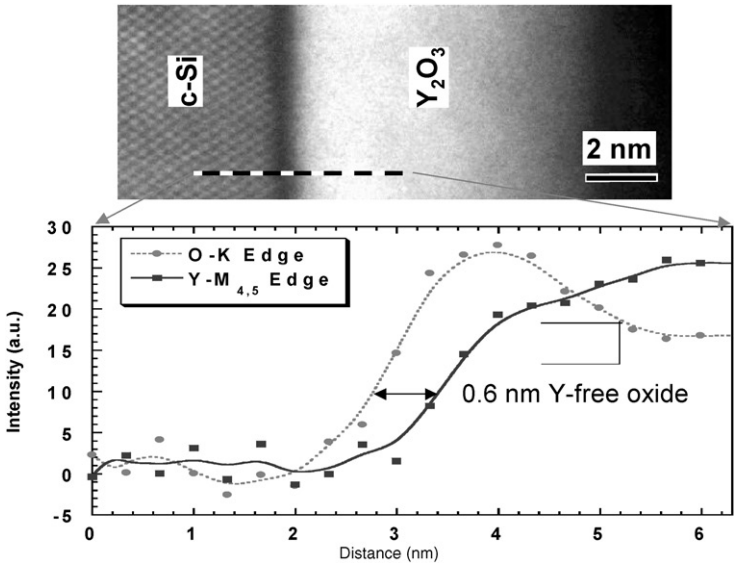

Fig. 5. Oxygen-K edge and yttrium-$M_{4,5}$ edge of EELS spectra for an a-Si/Y_2O_3/c-Si film, showing a SiH_xO_y hydroxide near the Si interface.

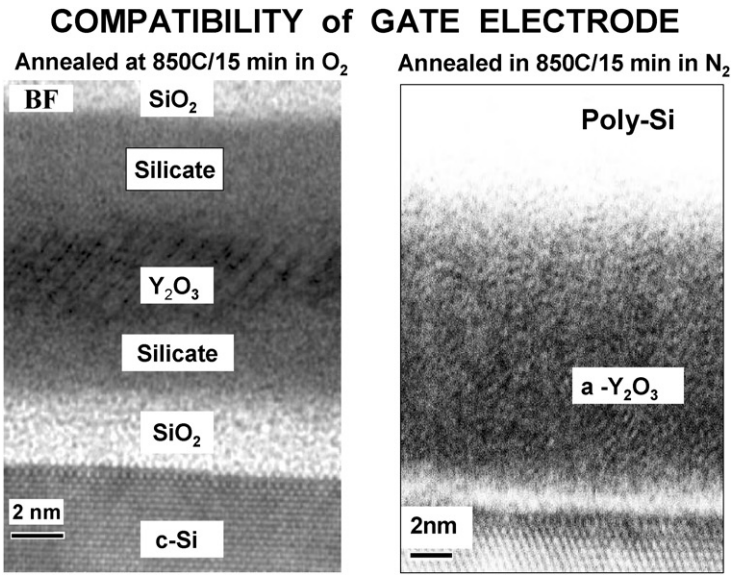

Fig. 6. BF-STEM cross sectional images for: (a) O_2 annealed, and (b) N_2 annealed a-Si/Y_2O_3/c-Si stacks at 850°C for 15 min.

substrate remained abrupt even after vacuum annealing to 900°C. Yttria layers are stable next to the amorphous capping Si up to 800°C, suggesting the good stability of yttria layers to the poly Si gate electrode.

Furnace anneals at 850°C under O_2 and N_2 atmosphere for 15 min were also performed for the a-Si/Y_2O_3/Si gate stacks, and the bright field (BF) cross-sectional STEM images are shown in Fig. 6(a), and (b), respectively. For the 850°C O_2 anneals, rapid diffusion of oxygen through the gate stack caused interfacial reactions and the formation of SiO_2 and yttrium silicate at both upper and lower interfaces. As for the 850°C N_2

anneals, the Y_2O_3 gate dielectric remained amorphous, and reacted very little with the amorphous Si gate electrode and the Si substrate. Both vacuum annealing and furnace annealing tests suggest that the rare earth oxides are compatible to the poly-Si electrode up to temperature as high as 850°C [16].

6. Conclusions

We have successfully employed the MBE-grown a-Si/Gd_2O_3/c-Si and a-Si/Y_2O_3/c-Si gate stacks with abrupt interfaces as a model system to elucidate critical processing integration issues. At the moment significant efforts are still needed to reach the goal of satisfactory replacement of the gate dielectric. Understanding of the electronic structure and the control of the electrical properties of the bulk of the dielectric and the dielectric/Si interface are essential to improve the reliability of these novel materials, before they can be fully integrated into CMOS processing.

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References

[1] G.D. Wilk, et al., J. Appl. Phys. 89 (2001) 5243.
[2] R.M. Wallace, G.D. Wilk (Eds.), Alternative Gate Dielectrics for Microelectronics, Materials Research Bulletin, 27(3) (2002).
[3] K.J. Hubbard, et al., J. Mater. Res. 11 (1996) 2757.
[4] M. Passlack, et al., IEEE Trans. Electron Dev. 44 (2) (1997) 214.
[5] M. Hong, et al., J. Crystal Growth. 175/176 (1997) 422.
[6] F. Ren, et al., Solid State Electron. 41 (11) (1997) 1751.
[7] Y.C. Wang, et al., IEEE Electron Dev. Lett. 20 (1999) 457.
[8] J. Kwo, et al., Appl. Phys. Lett. 75 (1999) 1116.
[9] M. Hong, et al., Appl. Phys. Lett. 76 (2000) 312.
[10] M. Hong, et al., Science 283 (1999) 1897.
[11] F. Ren, et al., IEEE Electron Dev. Lett. 19 (8) (1998) 309.
[12] M. Hong, et al., in: R. Kopf, A.G. Baca, S.N, G. Chu (Eds.), Compound semiconductor power transistors II and state-of-the-art program on compound semiconductors (SOTAPOCS XXXII), ECS Proceedings 2000–1, p. 103.
[13] J. Kwo, et al., unpublished.
[14] J. Kwo, et al., Appl. Phys. Lett. 77 (2000) 130.
[15] J. Kwo, et al., J. Appl. Phys. 89 (2001) 3920.
[16] B. Busch, et al., Appl. Phys. Lett. 79 (2001) 2447.
[17] B. Busch, et al., in: R.M. Wallace, G.D. Wilk (Eds.), Alternative Gate Dielectrics for Microelectronics, Materials Research Bulletin, 27(3) (2002) 206.
[18] S. Stemmer, J.-P. Maria, A.I. Kingon, Appl. Phys. Lett. 79 (2001) 102.