# High temperature stability in lanthanum and zirconia-based gate dielectrics

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Gate dielectrics composed primarily of lanthana and zirconia were prepared by reactive evaporation. The stability of the layers during high temperature anneals was investigated. By controlling the oxygen partial pressure during heat treatment, lanthana and zirconia films could be protected against reaction with the underlying Si substrate and against the growth of low-$\varepsilon$ interface layers. The electrical thickness of the dielectrics could be maintained after a 900 °C exposure. The critical oxygen pressure at 900 °C for low-$\varepsilon$ interface formation beneath $ZrO_2$ and $La_2O_3$ dielectrics was $\sim 2e^{-4}$ Torr. The interfaces that formed beneath the $ZrO_2$ and $La_2O_3$ layers are distinctly different. The sub-$ZrO_2$ interface, influenced primarily by phase separation, tends towards pure $SiO_2$, while the sub-$La_2O_3$ interface, influenced primarily by silicate formation, tends towards a La–Si–O alloy. For both materials, reducing the oxygen pressure to values below $10^{-7}$ Torr resulted in rapid degradation of the metal oxide. This dielectric degradation is believed to be linked to SiO evaporation. These results suggest that at high temperatures, a window of optimal oxygen partial pressure exists in which the stability of many oxides in contact with silicon can be achieved.  [DOI: 10.1063/1.1391418]

## I. INTRODUCTION

The reduction of complimentary metal oxide semiconductor (CMOS) device dimensions through transistor scaling is in part limited by the $SiO_2$ dielectric layer thickness. As the $SiO_2$ layer is thinned to provide increased capacitance density, leakage currents increase rapidly. Below ~30 Å at a given voltage, the leakage current increases by approximately 1 order of magnitude for each 2 Å reduction in thickness.[1–3] Currently, it is believed that the maximum allowable gate leakage currents will range between $10^1$ to $10^{-3}$ A/cm$^2$. The specific value will be application dependent. To ameliorate this problem, a higher permittivity layer may be substituted for $SiO_2$, and an equivalent capacitance density may be achieved in a physically thicker insulating layer. The thicker layers should in turn provide reduced leakage current values.

Replacing $SiO_2$, however, is nontrivial. Although literature examples citing low-leakage alternative gate dielectrics with capacitance densities equivalent to 10 Å of $SiO_2$ can be found, other important electrical parameters like flat band voltage and mobility have yet to be demonstrated at values consistent with similarly thin $SiO_2$ metal oxide semiconductor (MOS) transistors.[4–6] In part, this condition is caused by electrically active defects that are likely associated with the metal-oxide/semiconductor interface.[7,8] The nature of this interface is determined by interactions between the silicon substrate and the high-$\varepsilon$ dielectric. Presumably, deleterious film/substrate interactions are associated with potentially unwanted interface formation and greater concentrations of electrically active defects. As such, it is the intent of this investigation to determine the processing conditions providing the greatest Si/metal-oxide stability, especially as it pertains to high temperature anneals. In current transistor process flows, gate stacks must be exposed to temperatures as high as 1050 °C. This is primarily due to the need for rapid anneals which activate implanted dopant species. It is possible that process flows can be modified to reduce these aggressive treatments, but high temperature stability is clearly preferable. If clean interdiffusion free interfaces can be achieved, the most desirable electrical properties may be expected. This argument, however, ignores the possibility that abrupt metal-oxide/Si interfaces will be intrinsically defective. This is beyond the scope of this investigation, however, its importance is acknowledged.

Hubbard and Schlom have investigated gate dielectric stability by evaluating the thermodynamically preferred reaction products for metal oxides in contact with silicon at 1000 K.[9,10] Consequently, current researchers are concentrating on several materials with predicted stability. These selections include: $ZrO_2$, $HfO_2$, $La_2O_3$, $Y_2O_3$, $Al_2O_3$, and several of the associated silicates and aluminates.[11–23] We have attempted to build upon this work, specifically considering kinetic effects associated with oxygen transport through these thin layers. By combining the thermodynamic evaluations with kinetic considerations, it should be possible to improve interface stability, and to approach the electrical performance necessary for CMOS devices.

## II. EXPERIMENTAL PROCEDURE

Zirconia and lanthana gate dielectrics were prepared by reactive evaporation in an oxide molecular beam epitaxy

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(MBE) system. Lanthanum metal was evaporated from a high temperature effusion cell (W crucible) while zirconium was evaporated by electron beam heating. Both metals were deposited in the presence of molecular oxygen. The chamber pressure during deposition was 1.5 $e^{-5}$ Torr (the molecular beam approximation is appropriate for these conditions). Metal fluxes, measured during deposition by a quartz crystal monitor, were around $10^{14}$ atoms/cm$^2$ s. This is approximately 50 times lower than the oxygen impingement rate at this pressure thus considerable oxidation is expected after metal atom condensation. For this work, 150 and 200 mm uniformly doped ($10^{18}$/cm$^3$ boron) *p*-type silicon wafers were used, in all cases, the substrate temperature during deposition was 300 °C. The wafers were either HF dipped immediately before deposition, or a thin chemical oxide (J. T. Baker 111 solution) was grown and deposited upon.

Postdeposition processing consisted primarily of high temperature anneals. A rapid thermal annealer (Heatpulse 210) and a manufacturing scale vertical oxide growth furnace (Semitherm VT-1500) were utilized. The rapid thermal annealer (RTA) was operated in flowing nitrogen (atmospheric pressure) while the vertical growth furnace was operated between 0.2 and 200 Torr. In both furnaces, reagent grade nitrogen was used which contains ~1 ppm $O_2$. At atmospheric pressure, this provides an $O_2$ partial pressure of $7.6\times10^{-4}$ Torr, and corresponds to an impingement flux of greater than $\sim10^{17}$ molecules/cm$^2$ s. In the vertical furnace, the oxygen partial pressure was controlled by controlling the total nitrogen pressure. For example, the minimum pressure of the vertical furnace, 0.2 Torr, corresponds to an oxygen partial pressure of $2\times10^{-7}$ Torr.

MOS capacitor structures were made using Pt top electrodes. The Pt was deposited by magnetron sputtering (250 W, 100 mm target, 6 cm separation distance, and $3\times10^{-2}$ Torr Ar). The top electrode was patterned by lithography and liftoff. The capacitors were formed from 200 $\mu$m squares (capacitor sizes were within 2% of the nominally quoted values). The Pt sputtered electrodes were tested on high-quality thermal oxide. In doing so, it was determined that modest annealing (~400 °C 96%Ar/4%$H_2$) could remove defects associated with the sputter process. Transmission electron microscopy (TEM) analysis of similar structures annealed in $N_2$ at 400 °C suggests that interface reactions do not occur under these conditions.

Capacitance and leakage currents were measured as a function of voltage using a Hewlett Packard (HP) 4284A LCR meter and a HP 4145A semiconductor parameter analyzer. Backside contacts were made by scratching the wafer backside with a diamond scribe, then rubbing a high purity Al block across the scratches. This process effectively fills the scratches with aluminum and provides robust electrical connection to the silicon substrate. Several dot capacitors were selected on all samples and $C-V$ and $I-V$ measurements were made as a function of capacitor size and measurement frequency. This was performed to insure that the substrate doping was sufficient (in reference to the device capacitance), that backside contacts were reliable, and strong dielectric dispersion did not exist in the dielectric layers.

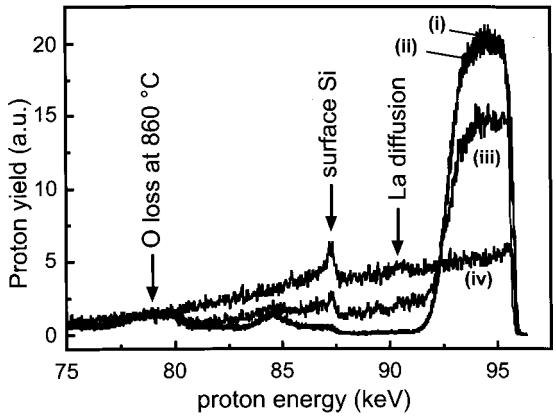


FIG. 1. MEIS spectra for a $La_2O_3\cdot SiO_2$ thin film deposited by reactive coevaporation. Spectrum (i) corresponds to the as-deposited state while spectra (ii) corresponds to the film after a vacuum ($10^{-8}$ Torr) anneal at 850 °C for several minutes. Degradation and decomposition of the film is evident from the high temperature anneal spectrum.

Select samples were characterized by TEM and medium energy ion scattering spectroscopy (MEIS).[24] Details of the specific procedures can be found in the references.

## III. RESULTS AND DISCUSSION

Evaluation of the available solid-state thermodynamic data indicates the stability of lanthana ($La_2O_3$) and zirconia ($ZrO_2$) in contact with Si at 1000 K. However, this stability is only expected under equilibrium conditions.[9,10] In practice, we must include the possibility of cases in which: (a) kinetics of the reaction processes are slow (equilibrium is not reached), (b) gas–solid reaction processes occur simultaneous to the solid state ones, and (c) impurities or imperfect stoichiometry influence the equilibrium condition. It is the gas–solid reaction processes that most confuse the simple picture and constitute the subject of this investigation. In one case gas-phase oxygen (or water) can add oxygen to the film, reacting to form $SiO_2$ either at the interface, or in the metal oxide (in the latter case as a silicate). In the second case, oxygen is lost from the film during high temperature anneals, leading to dielectric decomposition and the potential formation of a metal silicide. The actual mechanisms of oxygen loss are likely to involve the volatile SiO gas phase or the interface reaction which is known to produce it.[25] Both of these cases are discussed below, as well as a process to minimize the respective driving forces.

Figure 1 shows ion scattering (MEIS) spectra taken for a $La_2O_3\,SiO_2$ alloy deposited by coevaporation of La and Si in the presence of $O_2$ in the as-deposited state, and after an 800 °C, 840 °C, and 850 °C $10^{-8}$ Torr conventional vacuum anneal. The as-deposited film composition was $(La_2O_3)\cdot(SiO_2)$ which corresponds to the $La_2SiO_5$ crystalline silicate analog stoichiometry. Comparing the three spectra, the alloy decomposition can be clearly seen. The intense peak at ~94 keV in spectra (i) and (ii) signifies La confined to a discrete surface layer. In spectrum (iii), after vacuum annealing, the significant broadening of the La peak implies that the La has diffused and mixed with the Si substrate. After 860 °C exposure, this reaction is even more pronounced. Published ther-

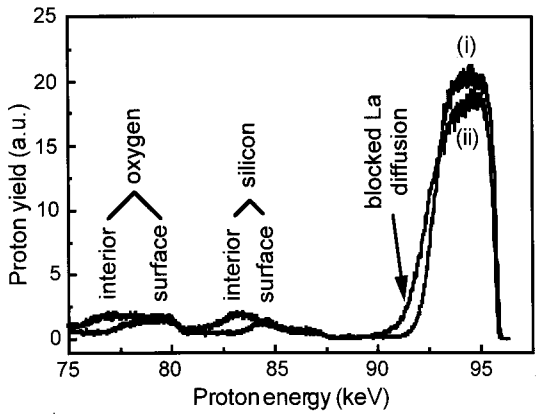


FIG. 2. MEIS spectra for a $La_2O_3 \cdot SiO_2$ thin film deposited by reactive coevaporation. Spectrum (i) corresponds to the as-deposited state while spectra (ii) corresponds to the film after air anneal at 850 °C for several minutes. Subgate dielectric silica growth is apparent on the after-annealed spectrum. Insets in the figure indicate increased subsurface oxygen and silicon signals.

modynamic data predict stability of lanthana (and a mixture of lanthana and silica) in contact with Si at these temperatures, however, from the figure it is apparent that the system is unstable under these conditions. It is likely that the observed decomposition occurs as a result of oxygen loss. Oxygen loss can occur via either direct La reduction from the lanthanum-containing layer, or via SiO desorption. The authors have previously observed evidence of SiO desorption from zirconia-alloyed silica;[26] that oxygen leaves the surface should not be considered anomalous. It is well know that ultrathin $SiO_2$ films on Si will desorb SiO in the 700–1000 °C range depending on the $SiO_2$ thickness and impurity concentration. SiO is isoelectronic with CO and unlike $SiO_2$, is stable in gas phase at elevated temperature. The reaction takes place at the interface: $Si_{(s)} + SiO_{2(s)} \Leftrightarrow 2SiO_{(g)}$, and with increasing silica thickness, the SiO desorption channel becomes more difficult to initiate. In the case of metal oxide overlayers on Si and $SiO_2$, the exact decomposition mechanism may be particularly complicated. One possibility is that the silicon diffuses into or through the metal oxide layer, and once reaching the surface, it can leave as $SiO_{(g)}$. The reaction would take place in conjunction with silicidation of the reduced metal; thus, $Si + MO_x \Leftrightarrow MSi_y + SiO_{(g)}$. Regardless of the mechanism, it is apparent that stability may not be achieved in these, or other oxygen-deficient annealing atmospheres.

The alternative situation can be seen in Fig. 2 where MEIS spectra are given for an identical film annealed to the same temperatures in air. From the spectra it is apparent that the decomposition discussed above does not occur. The important difference in the spectra is the increased width of the signals corresponding to oxygen and silicon; this increase occurs on the low energy side of the O and Si peaks, below the original silicate later indicating subsurface silica formation. In addition, the La spectrum itself is now broader (distributed deeper in the film). This could occur because of roughness in the overlayer or because some of the interfacial La has diffused down (or additional $SiO_2$ diffused up) making a more Si-rich lanthana silica alloy. This suggests that the La-containing film is stable, i.e., not susceptible to decomposition/silicide formation, but in the presence of oxygen can later react with an underlying silica. The films used in these experiments were 100 Å thick. For thinner films, it is likely that the temperature for subsurface oxide growth would be lower as transport through a thinner surface layer will occur more rapidly.

For the case of $ZrO_2$, literature data can be found indicating related behavior. Busch *et al.* examined the $ZrO_2/Si$ interface as a function of temperature and pressure and found that under oxidizing conditions, a subsurface $SiO_2$ layer rapidly grew with no change to the zirconia dielectric.[23] In this case, the growth rates of the subsurface oxide were considerably faster than otherwise suggested by Deal–Grove kinetic models.[27] Small but measurable interface oxidation occurred at 300 °C (for an oxygen pressure in the Torr range) and increased rapidly with increasing temperature. This was attributed to species other than molecular oxygen, i.e., atomic oxygen, diffusing through the dielectric layers to rapidly oxidize the silicon substrate. Busch's experiment establishes the high oxygen pressure limiting stability case. The low-pressure case has been originally investigated by Copel *et al.* and later by Kwong *et al.* through annealing zirconia films in vacuum ($10^{-8}$ Torr) as a function of temperature. The findings indicated that decomposition occurred between 800 and 900 °C.[21,28] MEIS and XPS measurements within this temperature range were interpreted as implying the conversion of zirconia to metallic zirconium and ultimately silicide. Corroborating decomposition results were also observed by Busch *et al.*[23] In Copel *et al.*'s and Kwong *et al.*'s investigations XPS and cross-sectional TEM also showed that interfacial silica formed when anneal conditions were oxidizing.

Considered together, these results demonstrate the limiting cases of stability for oxides in contact with silicon. The low pressure case indicates the propensity of a material to decompose at high temperatures (quite possibly aided by the presence of $SiO_{(g)}$) and subsequently react, while the oxidizing conditions suggest that thermodynamic stability is observed, but oxygen kinetics are such that subsurface silica growth is rapid. With this understanding, it should be possible to find an intermediate pressure at which oxide stability is maintained, and at which subsurface oxide growth is sufficiently slow as to minimize low-$\varepsilon$ interface formation. If such a pressure could be found, gate dielectric stability at high temperatures could be improved. Presumably, this temperature-pressure combination would be dynamic, which is to say that higher temperatures will require higher oxygen pressures. Granted, for some applications the gate dielectric is likely to be capped with a gate electrode in which case the oxygen partial pressure will be small. However, non-poly-Si gates, which will be required in future generations, may be poor oxygen diffusion barriers (especially if based on noble metals) and may not be integrated in a manner which protects the gate dielectric during high temperature heat treatments.

To investigate this engineered stability possibility, sets of lanthana and zirconia gate dielectrics were prepared and annealed at constant temperature, but as a function of oxygen

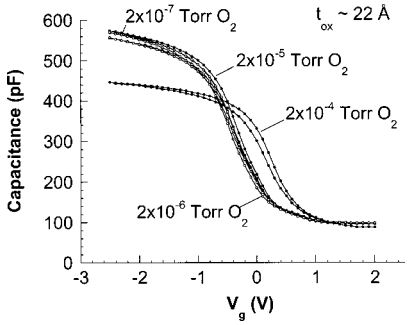


FIG. 3. Set of $C-V$ curves for a 20 Å thick $La_2O_3$ film deposited on (001) Si with an ~10 Å thick chemical $SiO_2$ interface. The $C-V$ curves correspond to samples exposed to a 900 °C anneal under oxygen partial pressures indicated in the figure. The large drop in capacitance observed with the $2\times10^{-5}$ Torr anneal suggests that at this pressure interfacial silica forms via oxygen diffusion.

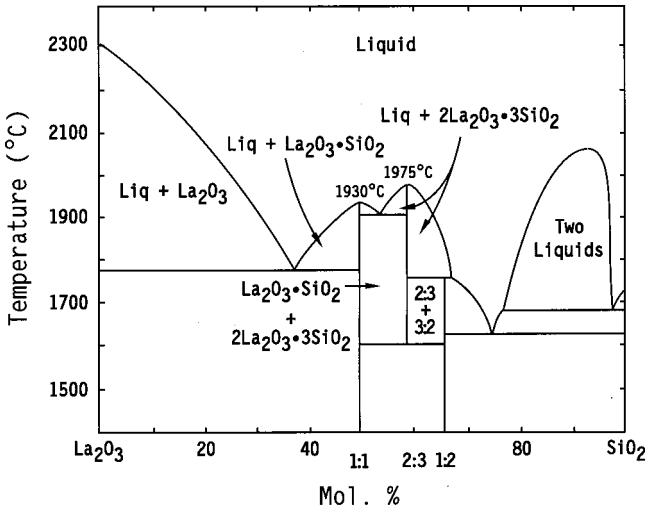


FIG. 5. Phase diagram for the $La_2O_3{\cdot}SiO_2$ binary system. Of interest is the low temperature stability of the $La_2O_3{\cdot}SiO_2$ and $La_2O_3{\cdot}2SiO_2$ phases and the congruent melting $La_2O_3{\cdot}SiO_2$ and $2La_2O_3{\cdot}3SiO_2$ (Ref. 33).

ambient as discussed in the experimental procedure. After this annealing step, electrical properties were measured from dot capacitors with Pt gate electrodes. Figure 3 shows the $C-V$ data for a 20 Å $La_2O_3$ film deposited on HF last and annealed to 900 °C for 5 min dwells at several oxygen partial pressures. At an oxygen partial pressure of $2\times10^{-4}$ Torr there is an obvious drop in the capacitance, as well as a shift in the $C-V$ trace. The drop in capacitance is associated with subsurface oxide formation, and subsequent reaction with the $La_2O_3$ to form a silicate. Note that in this case, the term silicate is not restricted to chemical compositions corresponding to stoichiometric silicate phases, but is generally applied to an amorphous alloy between $SiO_2$ and $La_2O_3$.

In order to support this interface reaction hypothesis, additional $La_2O_3$ films were prepared and annealed under oxidizing conditions that promote subsurface silica formation. In this case, 20–30 Å $La_2O_3$ films were deposited on thermal oxide surfaces (grown *in situ* prior to lanthana deposition) and annealed to 800 and 900 °C for 30 s in flowing nitrogen (in the RTA furnace). Both as-deposited and as-annealed samples were measured by MEIS. Figure 4 summarizes the MEIS results and as seen in the figure, after exposure to high temperatures in an oxidizing ambient, reactions occur resulting in alloy formation. From these measurements, a reaction model is proposed which can accommodate

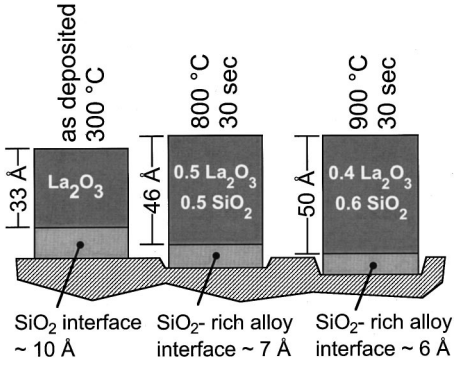


FIG. 4. Illustration depicting results of MEIS measurements on 20 Å lanthana films deposited on a thin chemical oxide. After exposure to high temperatures in an oxidizing environment, formation of silicate is observed.

the predicted thermodynamic stability of lanthana in contact with Si and the observations of reactions from MEIS. A critical aspect of this mechanism is that the originally deposited lanthana film does not react with silicon, rather, it reacts with a subsurface silica layer. This silica layer forms by oxygen diffusion through the $La_2O_3$ film. After this thermal oxidation, the $La_2O_3$ layer is in contact with $SiO_2$, and silicate formation must be considered. Tabulated thermodynamic data are unavailable for the lanthanum silicate crystalline phases, however, examination of the phase diagram for the $La_2O_3$–$SiO_2$ binary system can provide some insight. Figure 5 shows a representation of the published phase diagram for this system. The features of primary interest are the line compositions corresponding to $La_2O_3{\cdot}SiO_2$ and $La_2O_3{\cdot}2SiO_2$. These line compositions extend to low temperatures and melt congruently. This suggests that at the anneal temperatures used, depending on the quantity of silica present, the silicate phases would be thermodynamically preferred, and the congruent melting would insure that no kinetic limitation would exist to impede phase formation or mixing. If, for example, the silicate phases formed via a peritectic reaction, kinetic limitations from slow solid state diffusion may thwart the energetically preferred reactions.[29]

From these considerations it is possible to explain the drop on capacitance in Fig. 3 by interface formation and subsequent reaction. It is important to note that for oxygen pressures between $2\times10^{-7}$ and $2\times10^{-5}$ Torr, no changes are observed in the capacitance density. This suggests that within this pressure window, an oxygen partial pressure sufficient to cause interfacial oxide growth at rates important to the time scales of interest does not exist. This result suggests that stability can be achieved in these systems, provided that pressure is carefully controlled. At this point it has only been demonstrated that capacitance density falls after annealing in $10^{-4}$ Torr $O_2$ at 900 °C through interface formation. To insure that significant damage did not occur to the dielectric layer between $10^{-7}$ and $10^{-5}$ Torr anneals, it is useful to compare leakage current measurements. Figure 6 gives $I-V$

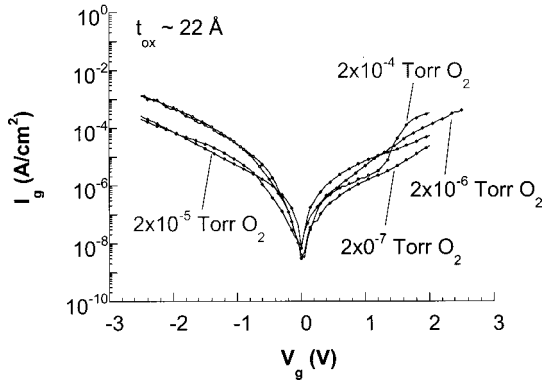


FIG. 6. Set of $I-V$ curves for a 20 Å thick $La_2O_3$ film deposited on (001) Si with an ~10 Å thick chemical oxide interface. The $I-V$ curves correspond to samples exposed to a 900 °C anneal under oxygen partial pressures indicated. That the leakage does not increase under the low pressure anneal conditions suggests that degradation of the dielectric is not occurring.

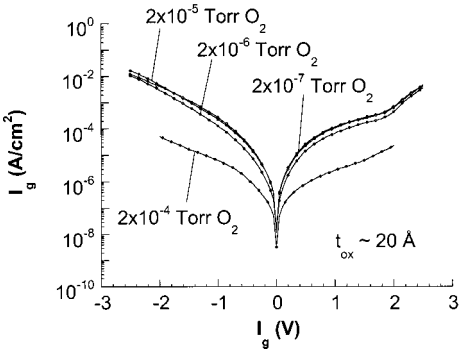


FIG. 8. Set of $I-V$ curves for a 20 Å thick $ZrO_2$ film deposited on (001) Si with an ~10 Å thick chemical oxide interface. The $I-V$ curves correspond to samples exposed to a 900 °C anneal under oxygen partial pressures indicated. That the leakage does not increase under the low pressure anneal conditions suggests that degradation of the dielectric is not occurring.

curves for the annealed lanthana samples. The leakage current does not increase for samples annealed at pressures below that at which a capacitance decrease was observed. This suggests that degradation of the dielectric layer did not occur. However, it must be noted that for the case of anneals producing reduced capacitance density, the leakage does not drop as would be expected for a physically thicker dielectric. This behavior is not well understood, but the authors conjecture that the physically thicker layer in this case corresponds to a silicate incorporating a large concentration of electrically active defects. Such a defective layer is one possibility that can explain the large leakage currents. The possibility of film roughening during this anneal must also be considered as a potential source of this higher-than-expected leakage. Recent results published by Chambers *et al.* and Guha *et al.* corroborate this proposed behavior.[20,22]

The same set of experiments was performed on zirconia films deposited on the same thin interfacial oxide surface. Again, samples were annealed to 900 °C as a function of oxygen pressure. As previously done, electrical measurements were taken from dot capacitors fabricated after the high temperature anneals. Figures 7 and 8 show the $C-V$ and $I-V$ measurement results. In this case, the behavior of zirconia is very similar to $La_2O_3$ in that the critical oxygen partial pressure for reduced capacitance is $\sim 2\times10^{-4}$ Torr. In the case of zirconia, however, the drop in capacitance is attributed to simple subsurface oxide formation, rather than reaction to form silicate. The leakage currents in this case are consistent with the $C-V$ analysis. A significant drop in leakage current density is observed at the oxygen pressure anneal that results in reduced capacitance density. It is proposed that the same oxygen diffusion occurs to produce a $SiO_2$ interfacial layer, however, this combination tends to favor a phase separated layer structure rather than a homogeneous (or graded) silica–zirconia layer. Again, in comparison to the lanthana case, growth of a relatively pure silica interface rather than a potentially defective silicate interface is more consistent with the observation of reduced leakage. Behavior identical to the proposed model, i.e., silica rather than silicate interface formation was documented by Garfunkel *et al.*, Copel *et al.*, Sun *et al.*, and Lee *et al.*[14,16,21,23] This behavior can be explained again by the published phase diagram for the $ZrO_2 \cdot SiO_2$ system, a representation of which is given in Fig. 9.

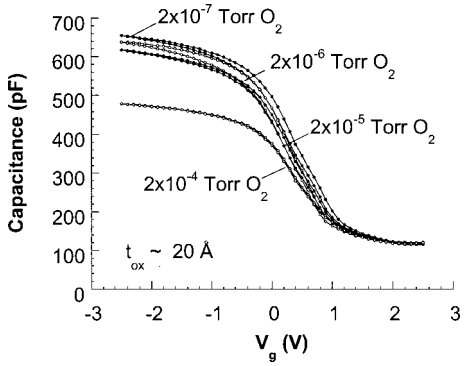


FIG. 7. Set of $C-V$ curves for a 20 Å thick $ZrO_2$ film deposited on (001) Si with an ~10 Å thick chemical $SiO_2$ interface. The $C-V$ curves correspond to samples exposed to a 900 °C anneal under oxygen partial pressures indicated in the figure. The large drop in capacitance observed with a $2\times10^{-4}$ Torr anneal suggests that at this pressure interfacial silica forms via oxygen diffusion.

The most important feature of this phase diagram is the peritectoid reaction required to form zirconium silicate upon cooling. This type of reaction requires that solid state diffusion of both Si and Zr atoms occur through highly refractory solids to form a new crystalline phase. From such a reaction, metastability will usually be expected. In addition, above the temperature of silicate formation, a two-phase region of zirconia and crystoballite spans the entire compositional range. This type of behavior indicates a propensity for both chemical segregation and phase separation for a zirconium silicate in the amorphous (or liquid) and crystalline phases (upon heating), respectively. Combined, these two factors indicate that true silicate formation will be kinetically difficult. This hypothesis is further supported by sintering studies of naturally occurring zircon powders. Curtis found that at temperatures several hundred degrees below the peritectoid reaction, decomposition of zircon to zirconia and silica occurred.[30] This model may initially appear to be in contrast to the work of Wilk *et al.* where zirconium silicate films were prepared

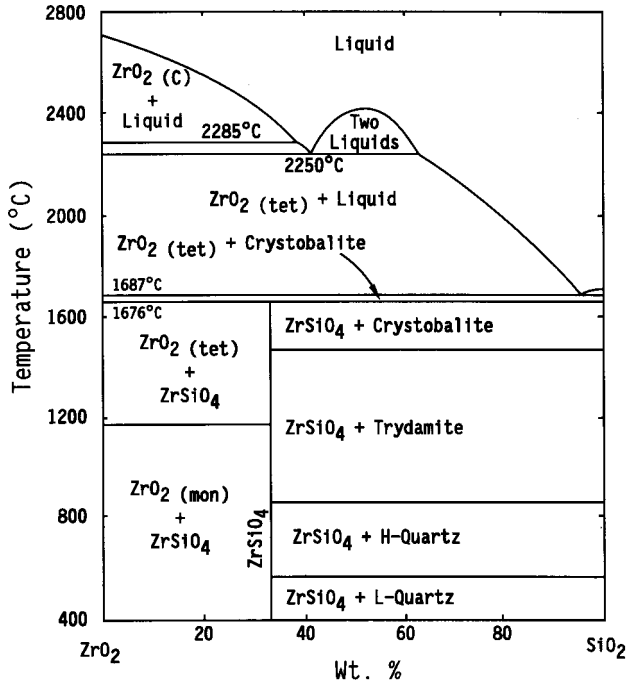


FIG. 9. Phase diagram for the $ZrO_2$–$SiO_2$ binary system. Of interest is the peritectoid reaction resulting in stoichiometric $ZrSiO_4$ and the two-phase region of $ZrO_2$+crystobalite spanning the entire compositional range (see Ref. 34).

by sputtering and found able to withstand high temperature anneals.[18] However, the concentrations of Zr in those samples was ~4%. It is likely that at such low Zr concentrations solubility could be maintained and multiple phases or other chemical heterogeneities would not be observed. Following these arguments, it is most likely that the drop in capacitance observed at the highest partial pressure resulted from subsurface oxide growth. Note that this mechanism is distinctly different from the results of lanthana film analysis.

Upon comparison, one important difference can be appreciated between the electrical data for lanthana and zirconia. For the electrode/substrate combination used, a flat band condition of ~0.2 V is expected. However, in the case of lanthana films annealed at oxygen pressures not resulting in reduced capacitance, a flatband condition at approximately −0.3 V is observed. This indicates the presence of an internal field traditionally thought to be a consequence of trapped charge in the dielectric. For the cases of alternative dielectrics, however, additional possibilities can occur, for instance, simply the interface between a covalent semiconductor like Si and an ionic insulator like lanthana may result in interface dipole formation. Regardless of the specific mechanism, it is clear that significant flatband shifts are characteristic of these lanthana films. Such flat band shifts have been observed for $La_2O_3$ and $Y_2O_3$ films by Guha *et al.*[20] The directions of these shifts were consistent with this work. When, however, anneal conditions result in reduced capacitance, the flatband condition is routinely observed to approach its predicted value. In Fig. 3, the flatband voltage is very close to 0.2 V after the most oxidizing anneals. In this work, all flatband shifts were determined using the $C-V$ data fitting algorithm developed by Hauser.[31] We suggest that the growth of a silica rich interface under the oxidizing conditions is responsible for this observation. Thus in the case of anneals which do not dilute the capacitance, the interface between the lanthana film and Si is quite rich in La cations—this occurs as the original lanthana films consume the thin chemical oxide resulting in a La-rich silicate. After anneals at higher oxygen pressures, additional interfacial silica grows, and the entire film (especially the interface) becomes silica rich. This new interface is similar to a pure $SiO_2$ interface, thus a flatband condition similar to the ideal situation is expected.

With regards to flatband voltage shifts in lanthana-based films, similar observations are not made for zirconia gate dielectrics. The flatband condition for these samples is ~0.2 V (the expected value) after all anneals. It is possible to interpret this observation in the context of the suspected reaction mechanism. The premise that a Zr-rich silicate interface does not form between $ZrO_2$ and Si under oxidizing anneal is consistent with these data. If the interface between zirconia and Si was relatively pure $SiO_2$, and the constitution of this interface did not change with different anneal conditions, changes in the flatband conditions would not be expected—this was experimentally observed.

## IV. SUMMARY AND CONCLUSIONS

Candidate alternative gate dielectric materials based on lanthana and zirconia metal oxides were investigated. Specifically, the stability of these materials in contact with silicon at high temperatures as a function of oxygen partial pressure was studied. The range of the temperatures and pressures used was established by expectations of future transistor processing flows. Two detrimental cases were observed. In the low pressure scenario (~900 °C/$10^{-8}$ Torr) the gate dielectric decomposed, while in the high pressure limiting case (>800 °C/$10^{2}$ Torr) a lower-permittivity interface formed. These situations were experimentally demonstrated for $La_2O_3 \cdot SiO_2$ alloys, while a combination of literature and experimental data were used to demonstrate similar behavior for $ZrO_2 \cdot SiO_2$. From a thermodynamic perspective, the oxides investigated should be stable at the temperature and pressure combination used: equilibrium Richardson diagrams have been calculated to support this.[32] As such, to explain these results an additional factor is required. The authors propose that under the decomposition conditions SiO is evaporating from the Si interface may interact with the metal oxide overlayer. SiO, which is isoelectronic with CO may be similarly reducing and may contribute to the dielectric decomposition. Alternatively, all of the interfacial $SiO_2$ may decompose to $SiO_{(g)}$ leaving the metal oxide in contact with the Si substrate. In this case, considering gaseous reaction products, a Si-metal oxide instability may occur. Given these boundaries, intermediate conditions were investigated where stability could be maintained to high temperatures. This was accomplished by performing high temperature anneals as a function of oxygen partial pressure. Electrical analysis of MOS capacitors exposed to these anneal conditions were used to determine the pressure stability limits. The electrical

properties were correlated with physical characterization results (both in this study and from literature) and published phase equilibria. Using this information, models describing the interface behavior were proposed.

For both materials, stability was demonstrated at 900 °C at oxygen pressures between $2\times10^{-7}$ and $2\times10^{-5}$ Torr. The stability is supported by the maintenance of a constant capacitance density before and after high temperature exposure. Though, direct physical causality cannot be ascribed to all electrical property characteristics, the consistency between the structural analysis, the trends in processing conditions, and the electrical properties are compelling. In general, lanthana-based gate dielectric films exposed to high temperatures (at pressures not supporting rapid interface growth) are characterized by large and negative flatband voltage offsets. When pressures are increased to provide interface growth, the flatband offsets are reduced. For zirconia-based gate dielectrics, the flatband voltage is very close to the predicted value, and changes very little with oxidizing anneals that promote interface formation.

In view of these results, we propose the following model: The interface observed between Si and $La_2O_3$ (after a high temperature anneal) will contain a large concentration of La cations. This interface results from the propensity for silicate formation in the system. This silicate formation was observed experimentally, and is expected from analysis of bulk phase equilibria. After a sufficiently oxidizing anneal the La cation concentration of the interface and near interface regions become diluted. This reduced concentration is may be responsible for the flatband shift to expected voltage values. Alternatively, the reaction mechanisms proposed for zirconia suggest that an interface rich in Zr cations will be unlikely after exposure to high temperatures. Consequently, the interface-determined electrical properties will resemble those of $SiO_2$/Si. The independence of flatband voltage on high temperature anneal conditions is probably a direct outcome of this behavior.

Finally, the authors maintain that published phase diagrams can be used to predict the behavior of other metal oxides in contact with silicon. In general, nonreactive metal oxides with congruently melting silicates like $Y_2O_3$, $Dy_2O_3$, $Gd_2O_3$, and $Er_2O_3$ will behave like $La_2O_3$. Alternatively, nonreactive metal oxides without silicates like BeO and $UO_2$ and metal oxides with peritectic silicates like $HfO_2$ and $ThO_2$ will behave like $ZrO_2$.

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