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# Synthesis of Polymer Dielectric Layers for Organic Thin Film Transistors via Surface-Initiated Ring-Opening Metathesis Polymerization

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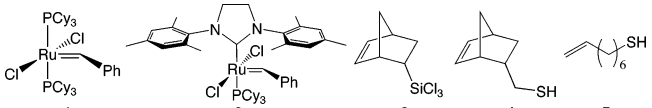
The use of organic materials in electronic devices such as field effect transistors (FETs) and light emitting diodes (LEDs) has become an attractive approach to decrease weight and cost, simplify production, and increase versatility of these devices. Electronic devices containing polymer layers have been incorporated into applications such as active matrix displays[1] and integrated circuits.[2]

For optimal FET performance, a polymer dielectric layer should be chemically and electrically compatible with the organic semiconductor, facilitating a smooth interface between adjacent layers.[3] Low leakage and tunable dielectric properties are also desirable. This requires that the layer be pinhole-free, with controlled thickness and composition.

Current methods for depositing polymer layers include spin-coating, ink-jet printing, and screen printing.[4] Unlike these methods, surface-initiated polymerizations can produce densely packed, conformal layers over any surface topology. Compared with other surface-initiated polymerization methods, ring-opening metathesis polymerization (ROMP) allows mild conditions and short reaction times. Therefore, we have chosen to investigate surface-initiated ROMP (SI-ROMP) as a method for forming polymer dielectric layers.

SI-ROMP has been demonstrated on Au, Si, and Si/$SiO_2$ surfaces using catalyst **1** and a variety of linking molecules.[5] Conformal block copolymers grown on Au nanoparticles demonstrated the living nature of SI-ROMP with catalyst **1**.[6] We report here that SI-ROMP polymer layers can be used as the dielectric layer in electronic devices, either alone or in tandem with an inorganic dielectric layer. We also report that, as with solution-phase ROMP,[7] catalyst **2** is more active than catalyst **1** in SI-ROMP.

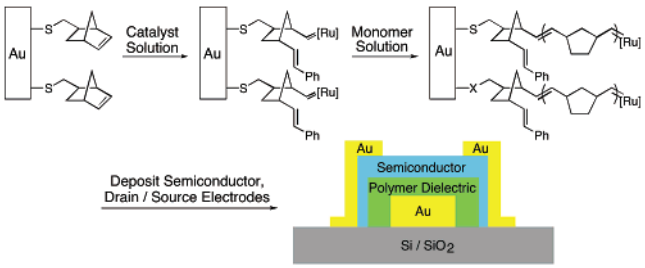



**1** **2** **3** **4** **5**

Polymer dielectric layers covalently attached to Au or Si/$SiO_2$ surfaces were formed via ROMP from surface-tethered metathesis catalysts (Scheme 1). Exposure of a self-assembled monolayer (SAM) of a linking molecule (**3**, **4**, or **5**)[8] to a solution of catalyst (**1** or **2**), followed by subsequent exposure to a solution of monomer, generated the polymer film. Between each of these steps, the surfaces were extensively rinsed with solvent to remove chemically unbound material.

Many variables were found to significantly affect the thickness and uniformity of SI-ROMP polymer films. Most importantly,

***Scheme 1.*** Construction of an FET Using an SI-ROMP Polymer Dielectric Layer (**4** Shown as Example Linker)




catalyst **2** is far more active than catalyst **1**. Given identical reaction conditions, films produced from catalyst **2** are up to 10 times thicker than those produced from catalyst **1**. For example, using **4** as the linker, films produced after 15 min of exposure to a 3 M solution of norbornene at room temperature are nearly 2.5 $\mu$m in thickness using catalyst **2**, versus 250 nm with catalyst **1**. Furthermore, catalyst **2** produces polymer films greater than 300 nm thick from 1 M monomer solutions, whereas catalyst **1** requires concentrations in excess of 3 M to produce equivalent films.

Polymerization conditions were also found to affect SI-ROMP films. Decreased thicknesses result for polymerizations conducted above room temperature or for prolonged periods of time (>1 h). Almost no film remains after 24 h of polymerization time, suggesting that, as in solution-phase ROMP, secondary metathesis (chain transfer) reactions are occurring between growing chains. Slower than ROMP and promoted by elevated temperature,[9] secondary metathesis in SI-ROMP would lead to chain termination and generation of polymer fragments that are no longer covalently attached to the substrate.

Smooth, pinhole-free dielectric films are important, since the overlaying semiconductor layer of an FET must continuously bridge the source and drain contacts.[10] Electrical shorting between the gate and drain and/or source electrodes was observed due to pinholes present in untreated SI-ROMP polynorbornene films. Annealing at 135 °C for 15 min densifies the films and significantly reduces the number of pinholes, resulting in relatively smooth, unshorted films.

Construction of FETs (as shown in Scheme 1) was demonstrated using the lamination method.[11] An SI-ROMP polymer dielectric layer was grown on an Au strip gate electrode (1000 Å thick, 1 mm wide) using linker **4**, catalyst **2**, and a 3 M norbornene solution. The thickness of the resulting polynorbornene film was 1.2 $\mu$m with a capacitance of 3 nF $cm^{-2}$ measured at 20 Hz. After annealing, a 400 Å layer of pentacene was vapor-deposited over the polymer dielectric. This was pressed against a separate PDMS substrate containing parallel Au strips as drain and source electrodes spaced 240 $\mu$m apart. A representative current−voltage ($I/V$) diagram for

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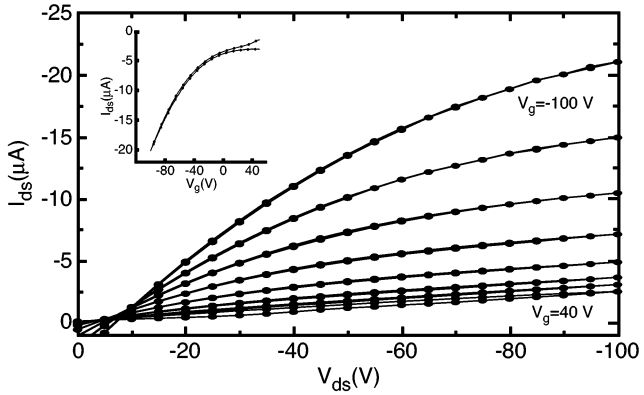


***Figure 1.*** Current−voltage characteristics of an FET produced by lamination, containing an SI-ROMP polynorbornene dielectric layer. The drain bias was swept from 0 to −100 V and back at gate biases between 40 and −100 V in −20 V steps. Inset shows drain current as gate voltage was swept from 40 to −100 V and back.

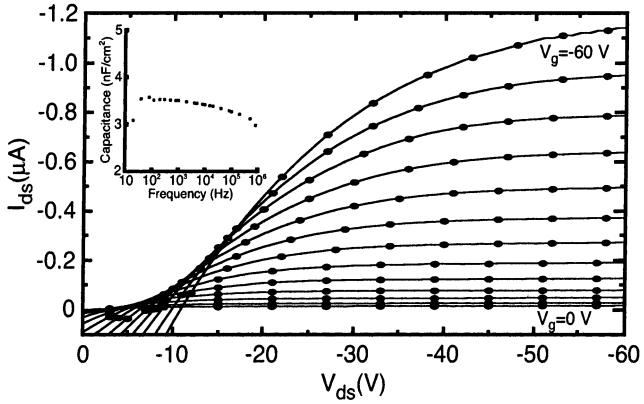


***Figure 2.*** Current−voltage characteristics of an FET produced by direct deposition of the semiconductor layer and Au drain/source electrodes over an SI-ROMP polynorbornene dielectric layer grown from a Au gate electrode. The drain bias was swept from 0 to −60 V at gate biases between 0 and −60 V in −5 V steps. Inset shows capacitance of a polynorbornene capacitor as a function of frequency. The leakage current is due to the unpatterned gate and organic semiconducting layers.

the resulting FETs is shown in Figure 1. Ranges for mobility and on/off ratio were 0.1−0.3 $cm^2\ V^{-1}\ s^{-1}$ and 10−100, respectively.[3] Little to no hysteresis was observed for these devices (see inset of Figure 1), indicating minimal charge buildup between the dielectric and semiconducting layers.

In addition to the lamination method, direct deposition of Au drain/source electrodes over the pentacene semiconducting layer also produced functioning FETs. Example *I*/*V* characteristics for these devices are shown in Figure 2. As seen in previous studies, mobilities and on/off ratios (up to $10^{-2}$ $cm^2\ V^{-1}\ s^{-1}$ and 100, respectively) were lower than those for the laminated devices due to partial degradation of the pentacene layer by the metal deposition.[11] The capacitance of the SI-ROMP dielectric films for these devices was found to have no significant frequency dependence down to 20 Hz (see inset of Figure 2).

Finally, FETs were constructed using an SI-ROMP polymer dielectric layer covalently bound to a $Si/SiO_2$ (either native or thermally grown oxide) surface. Working devices were constructed using either catalyst (**1** or **2**), linker **3**, and 2 M norbornene solutions.

Apart from washing extensively with solvent, no effort was made to remove residual (covalently bound or imbedded) catalyst from the polymer films. Rutherford backscattering spectroscopy (RBS) and medium energy ion scattering (MEIS) measurements, however, indicated very low surface concentrations of Ru for catalyst-functionalized SAMs as well as the washed films. Increasing the concentration of ruthenium bonded to the SAM may result in denser films and less leakage.

These devices demonstrate that surface-initiated polymer dielectric layers are both chemically and electrically compatible with other FET component layers. In general, a high yield (>90%) of working TFTs was obtained only with annealed dielectric films at least 1 μm thick. Further optimization of polymer growth conditions, yielding higher graft densities and reduced surface roughness, should allow the use of thinner films as well as improve the compatibility between the polymer film and organic semiconductor.[12]

For devices using patterned (e.g., striped Au) substrates, the SI-ROMP polymer grows conformally over the gate electrode, eliminating the need to pattern the dielectric. Furthermore, spin-coated dielectric layers tend to be thinner at the edges of the electrode, leading to a lower breakdown voltage. In contrast, the thickness of the surface-grown polymer layer can be about the same at the edges as for the flat surface, illustrating a clear advantage of SI-ROMP.

In conclusion, construction of FETs using SI-ROMP polymer dielectric layers has been demonstrated. Mild reaction conditions, short reaction times, and simple solution processing methods make SI-ROMP an attractive method for constructing polymer dielectric layers. Layer thicknesses ranging from below 100 nm to above 2 μm are accessible simply by varying the polymerization conditions. Research is underway in optimizing FET device characteristics, as well as incorporating SI-ROMP block copolymers into organic-based FETs.

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**Supporting Information Available:** Experimental details (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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(8) In general, films produced with linker **4** were thicker than those produced with linker **5**. Catalyst attachment is likely more efficient with **4**; the reasons for this are currently under investigation.

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(12) Increased grain size was observed when pentacene was deposited over SI-ROMP polymer layers that had been annealed.

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